100Gb/s CFP Optical Transceiver



Standards

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Ordering Information

Part No	Specifications				Application Code
	Pack	Data rate	Tx	Pout	Rx



Resistance					
Differential Resistance	Signal	Input	!	80	120

Lane					
Difference in Receive Power between Any Two Lanes		dBm	-	4.5	
Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm		-21.4	8
Receiver Sensitivity in OMA for Each Lane(OTU4)				-23.2	9
Stressed Receiver Sensitivity in OMA for Each Lane(100GbE)		dBm		-17.9	10&11
Los Assert		dBm	-30		
Los De-assert		dBm		-20.9	
Los Hysteresis		dBm	0.5		

Note1. The supply current includes CFP module's supply current and test board working current.

Note2. Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

Note4. Transmitter reflectance is defined looking into the transmitter

Note5. The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level

Note6. The average receive power , each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances

Note7. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

Note8. Receiver sensitivity (OMA), each lane (max) is informative

Note9. Measured with PRBS 2^{31}-1 for BER=10^{-5}. The BER for the OTU4 application is required to be met only after FEC has been applied.

Note10. Measured with conformance test signal at TP3 for BER=10^{-12}

Note11. conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins

Pin #	Symbol

Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins

Pin
#



Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is



8000	807F	RO	128	8	CFP NVR 1.Basic ID register
8080	80FF	RO	128	8	CFP NVR 2.Extended ID register
8100 8180	817F	RO	128	8	CFP NVR 3. Network lane specific registers



8010	1	RO	7~0	Transmitter Spectral Characteristics1		
8011	1	RO	7~0	Transmitter Spectral Characteristics2		
8012	2	RO	7~0	Minimum Wavelength per Active Fiber		
8014	2	RO	7~0	Maximum Wavelength per Active Fibe		
8016	2	RO	7~0	Maximum per Lane Optical Width		
8018	1	RO	7~0	Device Technology1		
8019	1	RO	7~0	Device Technology2		
801A	1	RO	7~0	Signal Code		
801B	1	RO	7~0	Maximum Total Optical Output Power per Connector		
801C	1	RO	7~0	Maximum Optical Input Power per Network Lane		
801D	1	RO	7~0	Maximum Power Consumption		
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode		

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold		
8082	2	RO	7~0	Transceiver Temp High Warning Threshold		
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold		
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold		
[redacted]	2	RO	7~0	VCC High Alarm Threshold		
808A	2	RO	7~0	VCC High Warning Threshold		
808C	2	RO	7~0	VCC Low Warning Threshold		
808E	2	RO	7~0	VCC Low Alarm Threshold		
8090	2	RO	7~0	SOA Bias Current High Alarm Threshold		
8092	2	RO	7~0	SOA Bias Current High Warning Threshold		
8094	2	RO	7~0	SOA Bias Current Low Warning Threshold		

		RW	7~0	Function Select Code		

A008

		RW	7~5	RX MCLK Control		
		RW	4	RX FIFO Reset		
		RW	3~1	RX Rate Select		
		RW	0	[illegible]		



			98	Module Fault Summary		

			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		



2	Reserved	

		RO/LH/COR	6	TX_HOST_LOL Latch		
		RO/LH/COR	5	RX_LOS Latch		
		RO/LH/COR	4	RX_NETWORK_LOL Latch		
		RO/LH/COR	3	Out of Alignment Latch		
		RO	2~0			

		RO	0	Initialize State Enable		
A029	1			**Module General Status Enable**		
		RW	15	GLB_ALRM Master Enable		
		RO	14	Reserved		
		RW	13	HW Interlock		
		RO	12~11	Reserved		
		RW	10	Loss of REFCLK Input Enable		
		RW	9	TX_JITTER_PLL_LOL Enable		
		RW	8	TX_CMU_LOL Enable		
		RW	7	TX_LOSF Enable		
		RW	6	TX_HOST_LOL Enable		
		RW	5	RX_LOS Enable		
		RW	4	RX_NETWORK_LOL Enable		
		RW	3	Out of Alignment Enable		
		RO	2~0	Reserved		





			13	Lane APD Power Supply Fault		
			12~8	Reserved		
			7	Lane TX_LOSF		
			6	Lane TX_LOL		
			5	Reserved		
			4	Lane RX_LOS		
			3	Lane RX_LOL		
			2	Lane RX FIFO error		
			1	Reserved		
			0	Reserved		
Network Lane FAWS Latch Registers						
A220	16	RO/LH/COR		**Network Lane n Alarm and Warning Latch**		
			15	Bias High Alarm Latch		
			14			



10 TX Power High Warning

A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value		
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value		
A2E0	32	RO	15~0	Reserved		

Table : CFP Pin-Map

PIN#	Top Row (2nd Half) Name	PIN#	Bottom Row (2nd Half) Name	PIN#	Top Row (1nd Half) Name	PIN#	Bottom Row (1nd Half) Name



25	TX_MCLKp	O	CML	For optical waveform testing. Not for normal use
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
28	VND_IO_D	I/O		Module Vendor I/O C. Do Not Connect
29	VND_IO_E	I/O		Module Vendor I/O C. Do Not Connect
30	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO. MSA Default: TRXIC_RSTn, TX&RX ICs reset,"0" Reset, "1" or NC: enabled=not used
31	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock LSB, "00""8W, "01" "16W, "10" "24W, "11" or NC"24W=not used
32	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock MSB, "00""8W, "01" "16W, "10" "24W, "11" or NC"24W=not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON."1":module power up completed,"0": module not high powered up
34				

41	GLB_ALRMn	O	LVCMOS	Global Alarm, “0” :alarm condition in any MDIO Alarm register, “1”: no alarm condition, Open Drain, Pull up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)

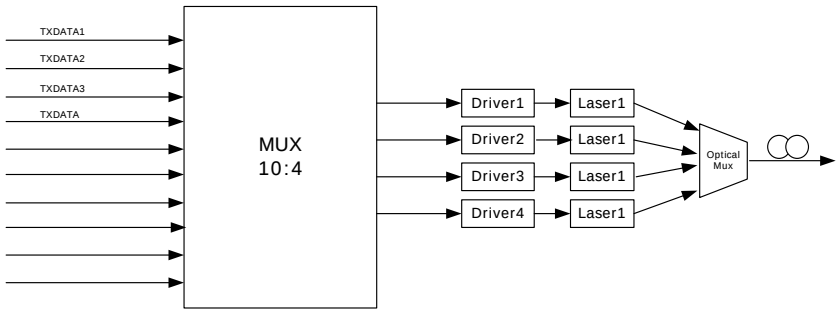


76	RX_MCLKp	O	CML	Receiver Monitor Clock (Optional)
77	RX_MCLKn	O	CML	Receiver Monitor Inverted Clock (Optional)
78	GND			
79	RX0p	O	CML	Output Data
80	RX0n	O	CML	Inverted Output Data
81	GND			
82	RX1p	O	CML	Output Data
83	RX1n	O	CML	Inverted Output Data
84	GND			
85	RX2p	O	CML	Output Data
86	RX2n	O	CML	Inverted Output Data
87	GND			
88	RX3p	O	CML	Output Data
89	RX3n	O	CML	Inverted Output Data
90	GND			

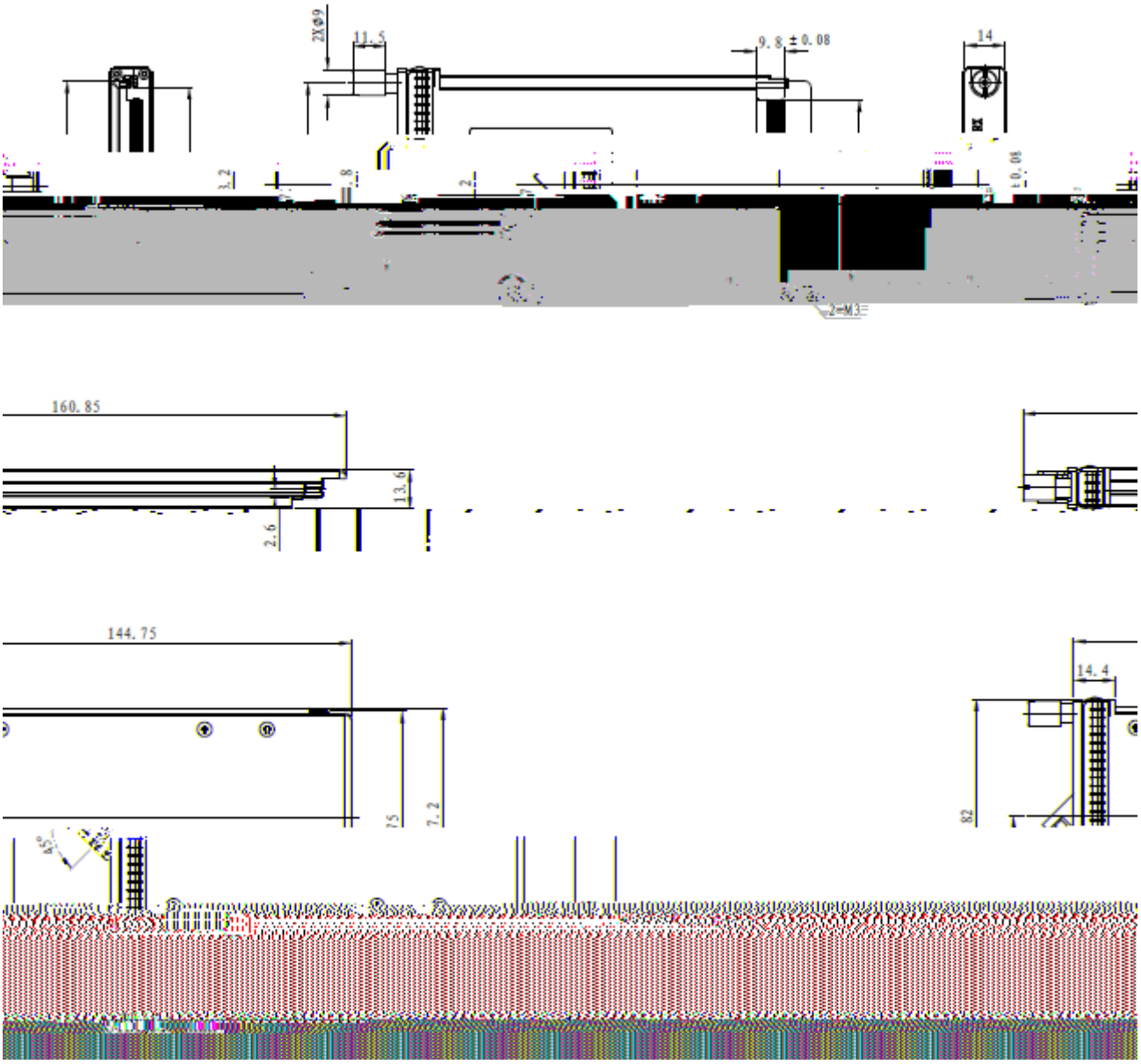
GN

outData N2 (ta)

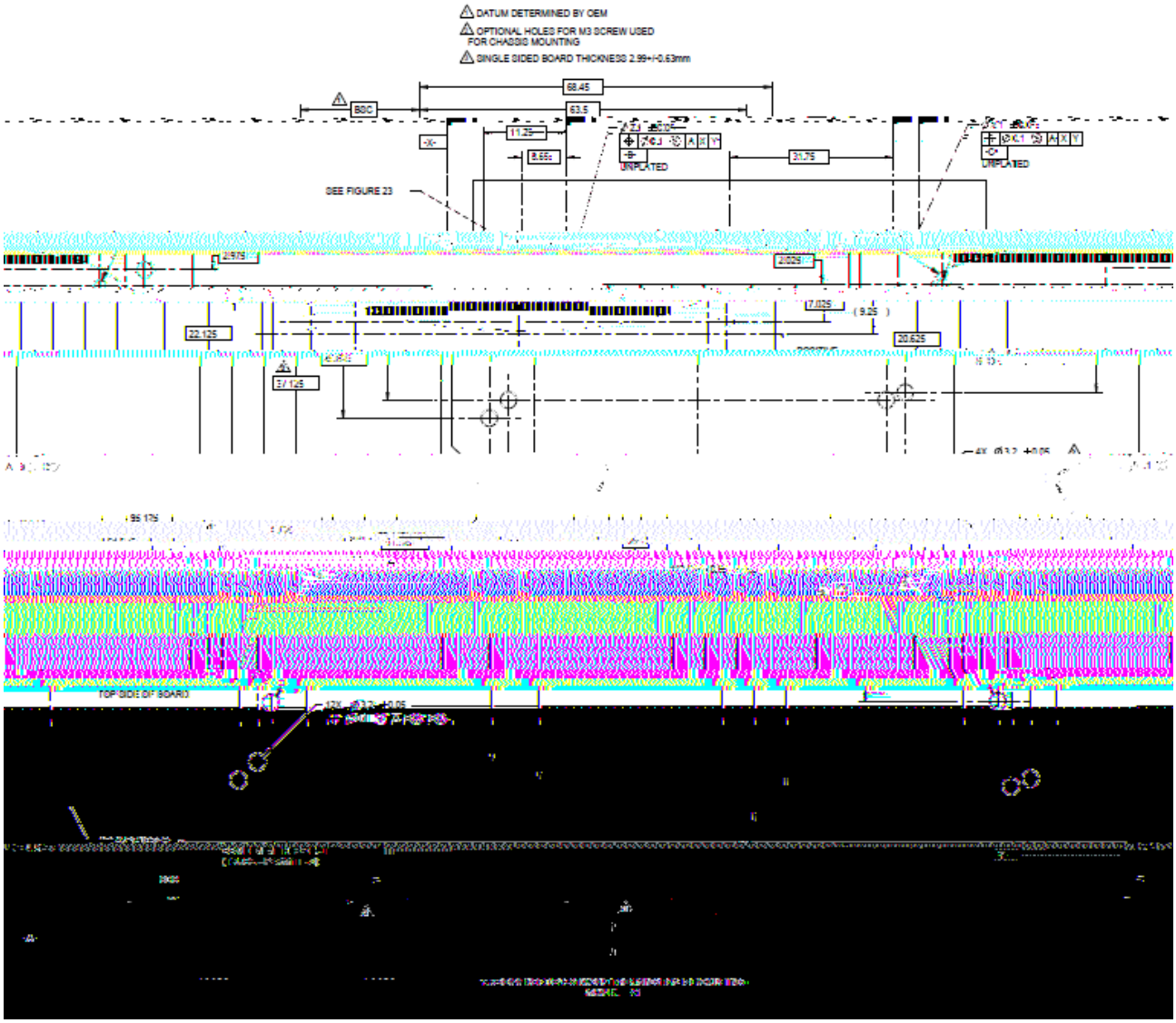
Block diagram



Package outline



PCB layout recommendation



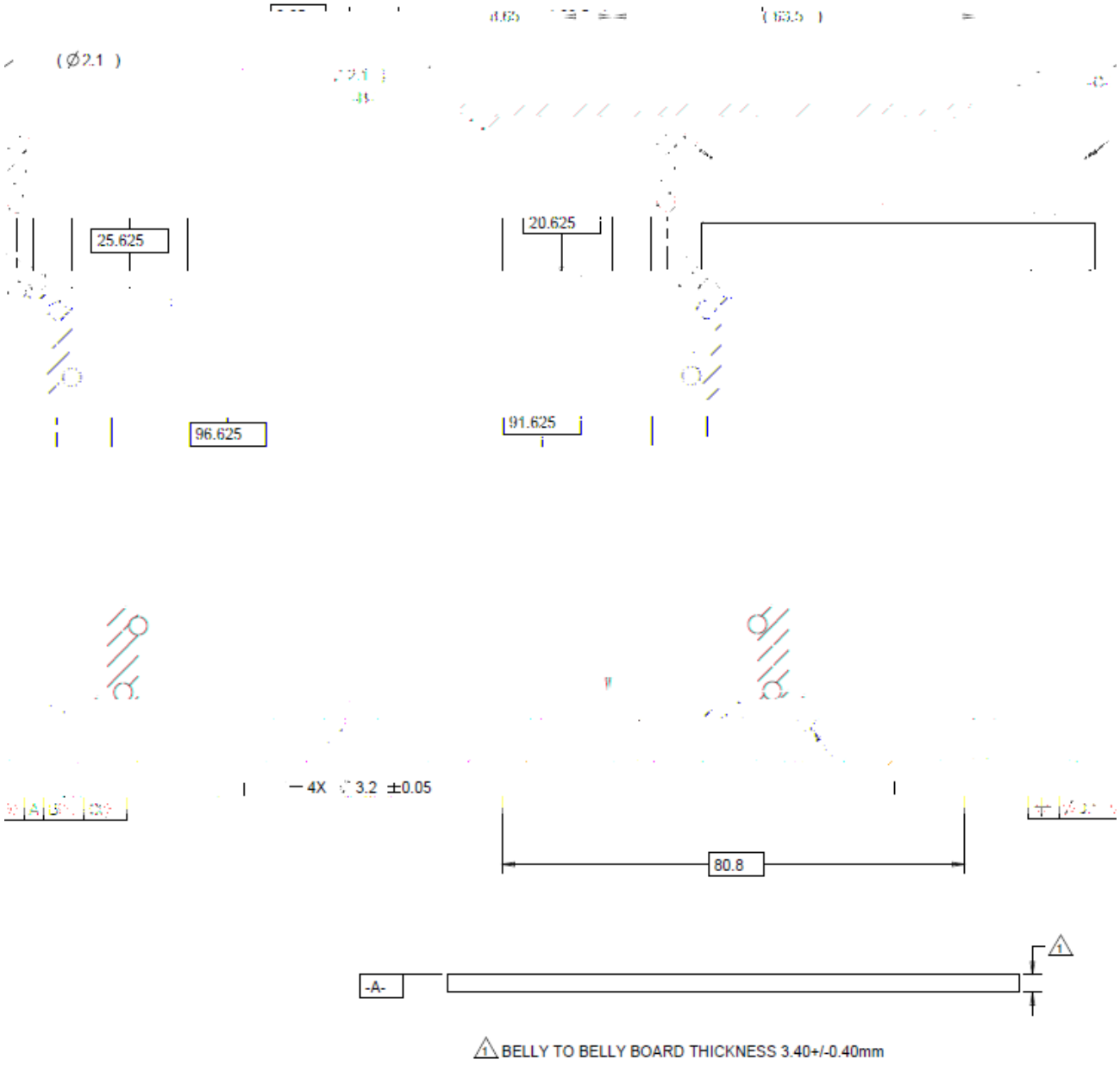

(Ø2.1)
25.625
96.625
20.625
91.625
4X Ø3.2 ±0.05
80.8
-A-
1
1 BELLY TO BELLY BOARD THICKNESS 3.40+/-0.40mm

FIGURE 21



Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins

	CENELEC
	EN55022
	VCCI Class 1